Sub. D1

1. (Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; [and]

a transistor provided on said planarized surface of said resinous layer[, said transistor comprising:] ; and

an interlayer insulating layer comprising resinous material provided over said transistor, said interlayer insulating layer having a leveling surface,

wherein said transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer amorphous silicon.

Sub. D2

5. (Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer [dielectric] insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer [dielectric] insulating layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said semiconductor layer comprises silicon and is obtained by crystallizing amorphous silicon.

C3 8. (Amended) The device of claim 5 wherein said interlayer [dielectric] insulating layer comprises polyimide.

11. (Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a transistor provided on said planarized surface of said resinous layer[, said transistor comprising:] ;and

an interlayer insulating layer comprising resinous material provided over said transistor, said interlayer insulating layer having a leveling surface,

wherein said transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises microcrystalline silicon.

12. (Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a transistor provided on said planarized surface of said resinous layer[, said transistor comprising:] ;and

an interlayer insulating layer comprising resinous material provided over said transistor, said interlayer insulating layer having a leveling surface,

wherein said transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises silicon and is obtained by crystallizing amorphous silicon.

18. (Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer[, and said thin film transistor comprising:] ;and

an interlayer insulating layer comprising resinous material provided over said thin film transistor, said interlayer insulating layer having a leveling surface,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises amorphous silicon.

22. (Amended) The device of claim 18 wherein said interlayer [dielectric] insulating layer comprises polyimide.

23. (Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer;

an interlayer [dielectric] insulating layer comprising a resinous material provided over said thin film transistor;

at least one pixel electrode provided on said interlayer [dielectric] insulating layer,

wherein said thin film transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises amorphous silicon.

25. 27. (Amended) The device of claim 23 wherein said interlayer [dielectric] insulating layer comprises polyimide.

28. (Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer[,];

an interlayer insulating layer comprising resinous material provided over said thin film transistor, said interlayer insulating layer having a leveling surface,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said channel formation region comprises microcrystalline silicon.

33. (Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer [dielectric] insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer [dielectric] insulating layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said semiconductor layer comprises microcrystalline silicon.

REMARKS

Applicant wishes to thank the Examiner for the very thorough consideration given the present application. The Examiner's Office Action of **March 16, 2000** has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a One (1) Month Extension of Time* which extends the shortened statutory period for response to **July 16, 2000**. Accordingly, Applicant respectfully submits that this response is timely filed.

Claims 1-8 and 11-37 were pending in the present application prior to the aforementioned amendment. By the above actions, claims 1, 5, 8, 11-12, 182-23, 27-28 and 33 have been amended. Accordingly, claims 1-8 and 11-37 are now pending herein, and, for the reasons set forth in detail below, are believed to be in condition for allowance.

Paragraph 3 of the Office Action objected to the specification as containing a minor informality. By the above action, the specification has been amended to correct this informality.

Paragraph 5 of the Office Action rejects claims 1-8 and 11-37 under 35 U.S.C. §103(a) as being unpatentable over ***Wakai et al.*** (Hereinafter "***Wakai***") in view of ***Takenouchi et al.*** (Hereinafter "***Takenouchi***"). This ground of rejection is respectfully traversed for the following reasons and favorable consideration is requested in view thereof.

The Applicant respectfully contends that the Office Action of **March 16, 2000** has failed to set forth a *prima facie* case of obviousness based upon the applied references, and that the present invention is patentably distinct over the prior art. It should be noted that